Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

**AMENDMENT**

**To the Claims:**

1. (previously presented) A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric layer within the first area;

forming a plurality of first openings in the dielectric layer within the first area; and

forming a first material layer over the wafer, wherein the upper surface of the first material layer has pits at locations over the first openings, and the first material layer is a high stress dielectric layer.

2. (original) The stress relieving method of claim 1, wherein the first area comprises a scribe line.

3. (original) The stress relieving method of claim 1, wherein the second area comprises a region for forming a die.

4. (original) The stress relieving method of claim 3, wherein the first area comprises a scribe line.

5. (original) The stress relieving method of claim 1, wherein the first area and the second area are both regions for forming a die.

6. (original) The stress relieving method of claim 1, wherein the step of forming first openings in the dielectric layer within the first area further comprises forming a plurality of second openings in the first dielectric layer within the second area at the same

time and then depositing material into the second openings to form a plurality of second material layers.

7. (original) The stress relieving method of claim 1, wherein the first opening is not deep enough to expose a film layer underneath the dielectric layer.

8. (original) The stress relieving method of claim 1, wherein the first opening exposes a film layer underneath the dielectric layer.

9. (cancelled)

10. (currently amended) A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that no circuits are formed within the first area, the first area comprising a scribe line, the second area comprising a region for forming a die, wherein there is no opening formed in the dielectric layer within the first area;

forming a first material layer over the wafer to cover the dielectric layer; and

forming a plurality of first openings in the first material layer within the first area.

11-14. (canceled)

15. (original) The stress relieving method of claim 10, wherein the first opening is not deep enough to expose the dielectric layer.

16. (original) The stress relieving method of claim 10, wherein the first opening exposes the dielectric layer.

17. (original) The stress relieving method of claim 9, wherein before forming the second dielectric layer over the wafer, further comprises:

forming a plurality of second openings in the dielectric layer within the second

area; and

depositing material into the second openings to form a plurality of second material layers.

18. (original) The stress relieving method of claim 10, wherein the first material layer is fabricated from a dielectric material or a metal material.

19. (cancelled)

20. (previously presented) The stress relieving method of claim 10, wherein the first material layer is a high stress dielectric layer.